1. A method of programming a field programmable gate array (FPGA), comprising:

providing an FPGA having connections for configuration programming data, a configuration clock and reset;

connecting data, data strobe and initialize lines of a specified interface from a host computer to the FPGA's connections for configuration programming data, configuration clock and reset respectively;

the host asserting the reset to clear the configuration memory;

the host clocking configuration data over the data lines into the FPGA using the data strobe line to clock the configuration clock, the configuration data incorporating design parameters for the specified interface so that the FPGA, once programmed, incorporates the specified interface; and

conducting bidirectional communications between the host computer and the configured FPGA using the specified interface.

2. The method according to claim 1, wherein the specified interface comprises an IEEE 1284 compliant interface.

3. The method according to claim 2, wherein the bidirectional IEEE 1284 compliant communication is carried out using extended parallel port (EPP) mode communication.

4. The method according to claim 1, further comprising conducting In-Circuit Emulation functions using the bidirectional communications.

5. A method of programming a field programmable gate array (FPGA), comprising:

providing an FPGA having connections for configuration programming data, a configuration clock and reset;

connecting data, data strobe and INIT lines of an IEEE 1284 connection from a host computer to the FPGA's connections for configuration programming data, configuration clock and reset respectively;

the host asserting the reset to clear the configuration memory;

the host clocking configuration data over the data lines into the FPGA using the data strobe line to clock the configuration clock, the configuration data incorporating design parameters for an IEEE 1284 interface so that the FPGA, once programmed, incorporates an IEEE 1284 interface; and

conducting bidirectional IEEE 1284 compliant communications between the host computer and the configured FPGA.

6. The method according to claim 5, further comprising conducting In-Circuit Emulation functions using the bidirectional IEEE 1284 compliant communications.

7. The method according to claim 5, wherein the bidirectional IEEE 1284 compliant communication is carried out using extended parallel port (EPP) mode communication.

8. A method of programming a field programmable gate array (FPGA), comprising:

providing an FPGA having connections for configuration programming data, a configuration clock and reset;

connecting data, data strobe and initialize lines of a specified interface from a host computer to the FPGA's connections for configuration programming data, configuration clock and reset respectively;

the FPGA receiving a reset signal to clear the configuration memory;

the FPGA receiving configuration data over the data lines, the configuration data incorporating design parameters for the specified interface so that the FPGA, once programmed, incorporates the specified interface; and

conducting bidirectional communications using the specified interface.

9. The method according to claim 8, wherein the specified interface comprises an IEEE 1284 compliant interface.

10. The method according to claim 9, wherein the bidirectional IEEE 1284 compliant communication is carried out using extended parallel port (EPP) mode communication.

11. The method according to claim 8, further comprising conducting In-Circuit Emulation functions using the bidirectional communications.

12. A method of communicating with a field programmable gate array (FPGA), comprising:

communicating over a communication interface to configure the FPGA to function according to a programmed configuration; and

carrying out communications over the communication interface to the FPGA functioning according to the programmed configuration.

13. The method according to claim 12, wherein the programmed configuration comprises operation as a virtual device under test in an In-Circuit Emulation system.

14. The method according to claim 12, wherein the programmed configuration comprises operation as a virtual microcontroller in an In-Circuit Emulation system.

15. The method according to claim 12, wherein the communication interface comprises an IEEE 1284 compliant interface.

16. A method of communicating with a field programmable gate array (FPGA), comprising:

a host computer communicating over a communication interface to configure the FPGA to act as a virtual microcontroller;

executing instructions on a microcontroller device in synchronization with the virtual microcontroller; and

the host computer communicating with the FPGA using the same communication interface used to configure the FPGA.

17. The method according to claim 16, wherein the communication interface comprises an IEEE 1284 compliant interface.

18. The method according to claim 16, wherein the FPGA is further configured to incorporate the communication interface.

19. A method of communication with a field programmable gate array (FPGA), comprising:

connecting a host computer to the FPGA using a communication interface;

programming a configuration into the FPGA, the configuration incorporating an implementation of the communication interface; and

carrying out non-programming communication between the host computer and the FPGA using the communication interface.

20. The method according to claim 19, wherein the communication interface comprises an IEEE 1284 compliant interface.

21. The method according to claim 19, wherein the configuration further incorporating a virtual microcontroller.

22. The method according to claim 21, wherein the virtual microcontroller executes instructions in synchronization with a microcontroller to carry out In-Circuit Emulation functions.

23. A method of communicating with an FPGA, comprising:

communicating over a parallel communication interface of an FPGA to configure the FPGA to act as a parallel port to receive data from a host computer system and to configure the FPGA to operate as a virtual microcontroller;

the parallel port of the FPGA receiving data and communicating control information, the virtual microcontroller operating in lock step with a microcontroller under test; and

commanding the FPGA with instructions from the host computer system using the communication interface that configured the FPGA.

24. The method according to claim 23, wherein the parallel port comprises an IEEE 1284 compliant parallel port.

25. The method according to claim 23, wherein bidirectional IEEE 1284 compliant communication is carried out using extended parallel port (EPP) mode communication over the parallel port.

26. The method according to claim 23, further comprising conducting In-Circuit Emulation functions using the parallel port.